REMARKS

Applicants respectfully request the Examiner's reconsideration of the present application as currently amended.

Claims 1-9, 18-22, and 26-30 are pending in the present application.

Claims 1-9, 18-22, and 26-30 are rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent No. 6,397,242 ("Devine").

Claims 1, 18, and 30 have been amended.

Claims 37-42 have been added.

Support for amended claims 1, 18, and 30 is found on page 8 of the specification and in Figure 3 of the drawings. Support for claims 37-42 is found on page 8 of the specification. No new matter has been added.

Claims 1-9, 18-22, and 26-30 are rejected under 35 U.S.C. §102(b) as being unpatentable over Devine.

Specifically, the Office Action mailed 3/12/2007 states in part that

> As per claims 1-9 and 18-22, and 26-30, Device (sic) teaches a method for performing virtualization, comprising; (sic) executing a plurality of input output instructions from an instruction stream during a single virtualization event and identifying an I/O instruction; and scanning the instruction stream to determine whether additional I/O instructions are present within an extent of instructions in the instruction stream. (Abstract, col. 5, Lines12-col. 6, Line 52, col. 10, Lines 51-59, col. 24, Lines 2-13. Figures 1-2, and 7-8)
>
> Devine teaches a virtualization system that employs a virtual machine monitor (VMM) on segmented-architecture computers. The VMM monitors a virtual machine (VM) emulating the computer architecture, and determines whether code executing on the VM may be executed in a direct execution environment (e.g., where the host processor may be set up with reduced privileges) or must be executed in a binary translation environment (e.g., when the virtual and underlying architectures

> mismatch). Device (sic) specifically teaches of monitoring a single virtualization event. (col. 1, lines 53-64, col. 11, lines 34-48, 24, lines 18-26, col. 25, lines 7-21)

(3/12/2007 Office Action, pp. 2-3).

Applicants submit that claims 1-9, 18-22, 26-30, and 37-42 are patentable under 35 U.S.C. §102(b) over Devine.

Devine discloses a virtual machine monitor (VMM) and a virtual machine (VM) that has at least one virtual processor and is operatively connected to the VMM for running a sequence of VM instructions, which are either directly executable or non-directly executable. The VMM includes both a binary translation sub-system and a direct execution sub-system, as well as a sub-system that determines if VM instructions must be executed using binary translation, or if they can be executed using direct execution. Shadow descriptor tables in the VMM, corresponding to VM descriptor tables, segment tracking and memory tracing are used as factors in the decision of which execution mode to activate. The invention is particularly well-adapted for virtualizing computers in which the hardware processor has an Intel x86 architecture (see Devine Abstract).

Applicants submit that Devine does not teach or suggest performing virtualization of an input output (IO) device by executing a plurality of IO instructions from an instruction stream during a signal virtualization event.

On the contrary, Devine discloses virtualization of a processor not an input output device (see Devine column 11, lines 51-58, column 13, lines 11-48, and column 25, lines 1-21).

Furthermore, the text cited by the Office in the Office Action mailed 3/12/2007 does not disclose executing a plurality of input output instructions. In fact, applicants submit that input output instructions are not referenced anywhere in the Devine, less the execution of a plurality of input output instructions during a single virtualization event. Applicants respectfully request that the Office clarify the relevance of the cited text to the claimed invention.

In contrast, claim 1 as amended states

> A method for performing virtualization, comprising:
> virtualzing an input output (IO) device by executing a plurality of IO instructions from an instruction stream during a single virtualization event.

(Amended Claim 1) (Emphasis Added).

Claims 18 and 30 include similar limitations. Given that claims 2-9 and 37-39 depend on claim 1, and claims 19-22, 26-29, and 40-42 depend on claim 18, it is likewise submitted that claims 2-9, 19-22, 26-29, and 37-42 are also patentable under 35 U.S.C. §102(b) over Devine.

Applicants further submit that Devine does not teach or suggest identifying an input output instruction and scanning the instruction stream to determine whether additional IO instructions are present within an extent of instructions in the instruction stream.

Devine only references the term "instruction stream" in column 23, lines 9-13. Devine discloses that "Binary translators achieve high speeds by converting an input instruction stream into a target instruction stream, and caching these translations so that the subsequent execution of the instruction stream can reuse the same target instruction sequence" (see Devine column 23, lines 9-13). Applicants submit that this is not equivalent to identifying an input output instruction and scanning the instruction stream to determine whether additional input output instructions are present within an extent of instructions in the instruction stream.

In contrast, claim 2 states

> The method of Claim 1, further comprising:
> identifying an IO instruction; and
> scanning the instruction stream to determine whether additional IO instructions are present within an extent of instructions in the instruction stream.

(Claim 2) (Emphasis Added).

Claim 19 includes similar limitations. Given that claims 3-9 depend on claim 2, claims 20-22 and 26-29 depend on claim 19, it is likewise submitted that claims 3-9, 20-22, and 26-29 are also patentable under 35 U.S.C. §102(b) over Devine.

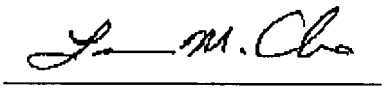
Claims 37-42 have been added to further define the virtualization event claimed in claims 1 and 18. Claims 37 and 40 describe the virtualization event to include having a virtual machine monitor emulate the IO instructions. Claims 38 and 41 describe the virtualization event to include storing a state of a processor of a virtual machine. Claims 39 and 42 describe the virtualization event to include reloading a stored state of a processor. Applicants submit that none of these aspects of a virtualization event is described in Devine.

In view of the amendments and arguments set forth herein, it is respectfully submitted that the applicable rejections and have been overcome. Accordingly, it is respectfully submitted that claims 1-9, 18-22, 26-30, and 37-42 should be found to be in condition for allowance.

The Examiner is invited to telephone Applicant's attorney (217-377-2500) to facilitate prosecution of this application.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,



Dated: July 12, 2007

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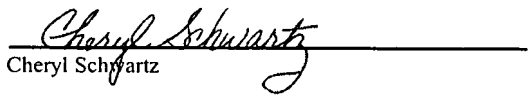
CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 12th day of July, 2007.



Cheryl Schwartz